WHAT IS CLAIMED AS NEW AND DESIRED TO BE SECURED BY LETTERS PATENT OF THE UNITED STATES IS:

1. A method for performing scan test on a semiconductor integrated circuit, said semiconductor integrated circuit comprising at least two blocks to be tested each capable of performing active functions, comprising the steps of:

isolating each of said at least two blocks to be tested exclusively from further blocks; and

supplying a plurality of scan clocks to each of said at least two blocks, said plurality of scan clocks each having a phase different from each other.

2. A semiconductor integrated circuit for use in a scan test operation, comprising:

at least two blocks to be tested each capable of performing active functions;

an isolation unit for isolating each of said at least two blocks to be tested exclusively from further blocks; and

an input terminal for inputting a plurality of scan clocks ~~each~~ to each of said at least two blocks, said plurality of scan clocks each having a phase different from each other.

3. The semiconductor integrated circuit according to claim 2, wherein each of said at least two blocks is provided with a Core Wrapper Architecture as said isolation unit.

4. The semiconductor integrated circuit according to claim 3, wherein

a Wrapper register included in said Core Wrapper Architecture is configured to be supplied selectively with one of a scan clock and a system clock for said blocks.

5. The semiconductor integrated circuit according to claim 4, further comprising:

an internal scan chain in each of said at least two blocks,

wherein

a shift enable signal for said Wrapper register is connected to a scan enable signal for said internal scan chain,

a clock for said Wrapper register is synchronous with a scan clock for said internal scan chain in said semiconductor integrated circuit, and

serial-in and serial-out terminals of said Wrapper register are each connected to an exterior of said semiconductor integrated circuit, so that an application of scan data from a tester and an observation of results obtained from a test of said application both become feasible.

6. The semiconductor integrated circuit according to claim 5, further comprising:

a logic built-in self test (BIST) in each of said at least two blocks,

wherein

serial-in and serial-out terminals of said Wrapper register are connected to an output of pseudo-random pattern generators (PRPG), and an input of multiple input serial register (MISR), of said logic BIST, respectively, each in parallel with said internal scan chain between said PRPG and said MISR.

7. A semiconductor integrated circuit capable of performing a scan test, the circuit comprising:

at least two blocks to be tested each capable of performing active functions;

an isolation unit for isolating each of said at least two blocks to be tested exclusively from further blocks; and

a clock generator for generating a plurality of scan clocks based on a clock input from an exterior controller, each clock generator to be supplied to each of said at least two blocks, said plurality of scan clocks each having a phase different from each other.

8. The semiconductor integrated circuit according to claim 7, wherein each of said at least two blocks is provided with a Core Wrapper Architecture as said isolation unit.

9. The semiconductor integrated circuit according to claim 8, wherein a Wrapper register included in said Core Wrapper Architecture is configured to be supplied selectively with one of a scan clock and a system clock for said blocks.

10. The semiconductor integrated circuit according to claim 9, further comprising:

an internal scan chain in each of said at least two blocks,

wherein

a shift enable signal for said Wrapper register is connected to a scan enable signal for said internal scan chain,

a clock for said Wrapper register is synchronous with a scan clock

for said internal scan chain in said semiconductor integrated circuit, and

serial-in and serial-out terminals of said Wrapper register are each connected to an exterior of said semiconductor integrated circuit, so that an application of scan data from a tester and an observation of results obtained from a test of said application both become feasible.

11. The semiconductor integrated circuit according to claim 10, further comprising:

a logic BIST in each of said at least two blocks,

wherein

serial-in and serial-out terminals of said Wrapper register are connected to an output of PRPG, and an input of MISR, of said logic BIST, respectively, each in parallel with said internal scan chain between said PRPG and said MISR.

12. A tester for applying a scan test on an integrated circuit, said tester comprising:

a circuit that isolates at least two blocks of an integrated circuit to be tested exclusively from further blocks of said circuit and supplies a plurality of scan clocks to each of said at least two blocks, said plurality of scan clocks each having a phase different from each other.

13. The tester of claim 12, wherein the integrated circuit further comprises an isolation unit and an input terminal for inputting said plurality of scan clocks to each of said at least two blocks.

14. The tester of claim 12, wherein the integrated circuit further.

comprises an isolation unit and a clock input for receiving said plurality of scan clocks at each of said at least two blocks.

15. A semiconductor integrated circuit capable of performing a scan test, the circuit comprising:

at least two block means to be tested each capable of performing active functions;

means for isolating each of said at least two blocks to be tested exclusively from further block means; and

terminal means for inputting a plurality of scan clocks ~~each~~ to each of said at least two block means, said plurality of scan clocks each having a phase different from each other.

16. The semiconductor integrated circuit according to claim 15, wherein each of said at least two block means is provided with a Core Wrapper Architecture as said means for isolating each of said at least two blocks to be tested.

17. The semiconductor integrated circuit according to claim 16, wherein a Wrapper register included in said Core Wrapper Architecture is configured to be supplied selectively with one of a scan clock and a system clock for said block means.

18. The semiconductor integrated circuit according to claim 17, further comprising:

internal scan chain means in each of said at least two block means, wherein

a shift enable signal for said Wrapper register means is connected to a scan enable signal for said internal scan chain means,

a clock for said Wrapper register means is synchronous with a scan clock for said internal scan chain means in said semiconductor integrated circuit means, and

serial-in and serial-out terminal means of said Wrapper register means are each connected to an exterior of said semiconductor integrated circuit means, so that an application of scan data from a tester means and an observation of results obtained from a test of said application both become feasible.

19. The semiconductor integrated circuit according to claim 18, further comprising:

logic BIST means in each of said at least two block means,

wherein

serial-in and serial-out terminals of said Wrapper register means are connected to an output means of PRPG, and an input means of MISR, of said logic BIST means, respectively, each in parallel with said internal scan chain means between said PRPG and said MISR.

20. A semiconductor integrated circuit capable of performing a scan test, the circuit comprising:

at least two block means to be tested each capable of performing active functions;

means for isolating each of said at least two block means to be tested exclusively from further block means; and

means for generating a plurality of scan clocks based on a clock

input from an exterior controller to be supplied to each of said at least two block means, said plurality of scan clocks each having a phase different from each other.

21. The semiconductor integrated circuit according to claim 20, wherein each of said at least two block means is provided with a Core Wrapper Architecture as said means for isolating each of said at least two blocks to be tested.

22. The semiconductor integrated circuit according to claim 21, wherein a Wrapper register included in said Core Wrapper Architecture is configured to be supplied selectively with one of a scan clock and a system clock for said block means.

23. The semiconductor integrated circuit according to claim 22, further comprising:

an internal scan chain means in each of said at least two block means,

wherein

a shift enable signal for said Wrapper register means is connected to a scan enable signal for said internal scan chain means,

a clock for said Wrapper register means is synchronous with a scan clock for said internal scan chain means in said semiconductor integrated circuit means, and

serial-in and serial-out terminal means of said Wrapper register means are each connected to an exterior of said semiconductor integrated circuit means, so that an application of scan data from a tester means and

an observation of results obtained from a test of said application both become feasible.

24. The semiconductor integrated circuit according to claim 23, further comprising:

a logic BIST in each of said at least two block means,

wherein

serial-in and serial-out terminals of said Wrapper register means are connected to an output means of PRPG, and an input means of MISR, of said logic BIST means, respectively, each in parallel with said internal scan chain means between said PRPG and said MISR.